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A Family of Active Switched Capacitor Biquad Building Blocks

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Two closely related, low-sensitivity, active switched capacitor filter topologies are presented. Each of these circuits comprises two operational amplifiers and at most nine capacitors. The topologies have been carefully constructed so that they are immune to the various parasitic capacitances normally present in switched capacitor networks. One filter topology is capable of realizing any stable biquadratic z-domain transfer function, while the second one is only slightly less than fully general. Most commonly used transfer functions can be realized with either topology and will require only seven capacitors. The choice between the two topologies will generally be made on the basis of total capacitance required, dynamic range behavior, and sensitivity. A complete set of synthesis equations is given for both circuits which cover both the general and all the important special cases of the biquadratic transfer function. Finally, several examples are given which illustrate the synthesis procedures and the versatility of the filter topologies.

I. INTRODUCTION

Active RC building blocks which realize a biquadratic transfer function[1,2] have played an increasingly important role in supplying filters for the Bell System. Thus, at the present time, STAR building blocks enjoy a very large volume of production and there is a constant effort directed toward the reduction of their costs.[3,4]

Perhaps the most promising recent development in filtering is the emergence of active switched capacitor filters.[5–8] These filters are fully MOS realizable and therefore enjoy the cost advantages of LSI integrated circuit realizations. Further, they can be expected to share in the future cost reductions due to VLSI.

Since biquadratic building blocks have played such a dominant role in the active RC field, they are also expected to be of great importance

for active switched capacitor (SC) filter realizations. Many of these basic biquadratic blocks can then be realized on a single chip to implement higher order filter functions.

The purpose of this paper is to describe a pair of similar active SC biquadratic filter topologies[9] capable of realizing any stable biquadratic z-domain transfer function. In arriving at these networks, we have been particularly careful to eliminate the effects of parasitic capacitances. Such capacitances arise mainly from two sources.

First is a sizable (approximately 10 percent) parasitic capacitance from the bottom plates of the capacitors to the epitaxial layer (ac ground). By using two operational amplifiers, it is possible to arrange matters so that the parasitic capacitors are connected either to a voltage source (operational amplifier output) or ground, thereby eliminating any effects due to them. Second are parasitic capacitances from the MOS switches to ground via the power supplies. By using only certain switching arrangements,[10] the parasitics again can be forced to appear at harmless locations.

After a description of the general biquad circuits, a full set of synthesis relations will be developed for them. The paper concludes with several examples that demonstrate the flexibility and general usefulness of these circuits.

II. GENERAL CIRCUIT TOPOLOGY

The transfer function of an active-RC biquad is biquadratic in the Laplace transform variable s:

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{cs^2 + es + d}{s^2 + as + b}. \tag{1}$$

In contrast, the active-SC biquad voltage transfer function is biquadratic in the z-transform[11] variable z, where $z = e^{sT_s}$ and T_s is the sampling interval, viz.,

$$\frac{V_{\text{out}}}{V_{\text{in}}}(z) = \frac{N(z)}{D(z)} = \frac{\gamma + \epsilon z^{-1} + \delta z^{-2}}{1 + \alpha z^{-1} + \beta z^{-2}}. \tag{2}$$

This is the general biquadratic transfer function we seek to realize. Of course, by suitable choice of the numerator coefficients, the different generic transfer functions, such as LP, BP, and HP, can be obtained.

All the filter topologies to be considered in this paper are special cases of the general active-SC biquad shown in Fig. 1a. This circuit bears a close resemblance to the three amplifier biquad;[2] however, because of the inversion[7] inherent in capacitor A, the inverter of the active-RC biquad is not needed. In effect, the circuit consists of two integrators, the first stage being inverting while the second stage is noninverting. Damping is provided by the capacitor E and the switched

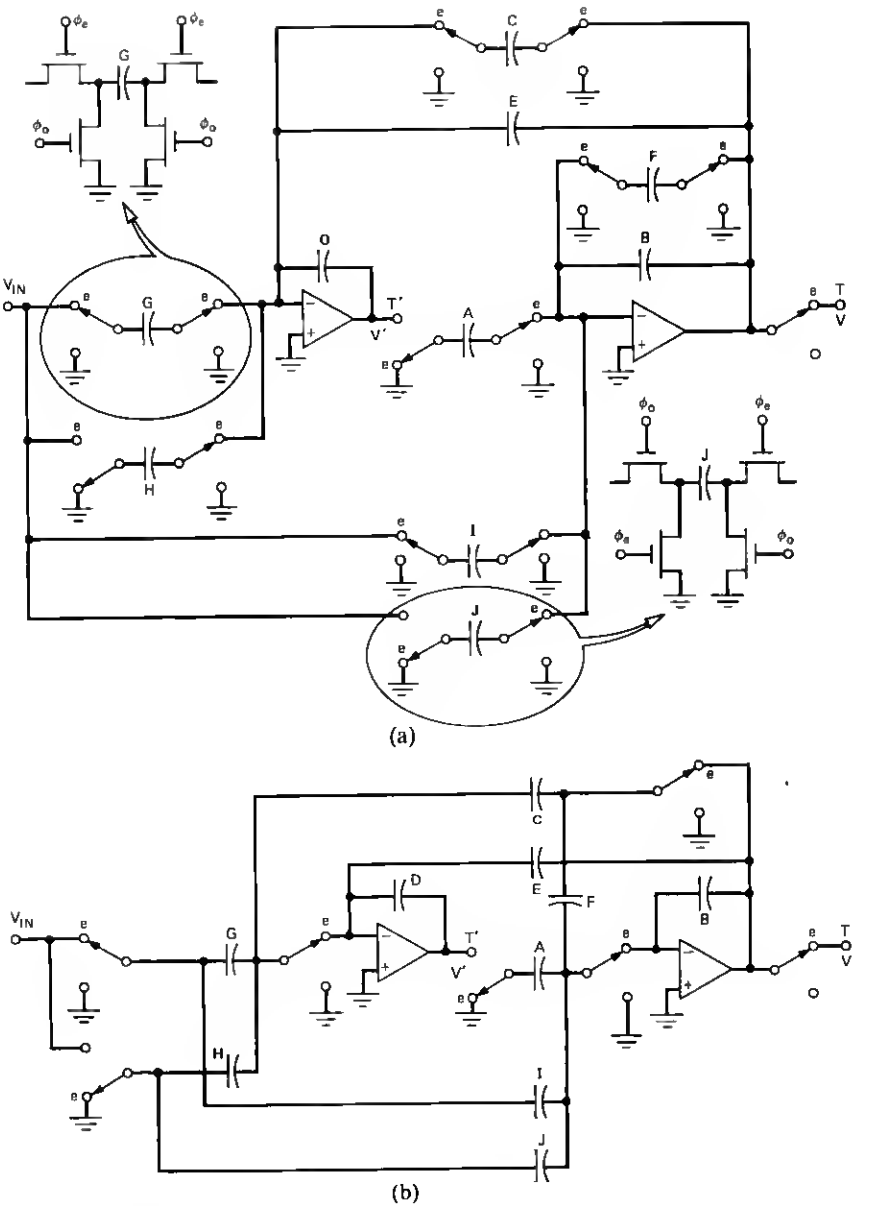


Fig. 1—(a) General active sc topology. (b) General active sc topology (minimum switch configuration).

capacitor *F*. In any particular application, only one of these will be present, leaving a total of nine capacitors, but for analysis purposes it is convenient to handle the two cases together.

The transmission zeros are realized via the multiple feed-forward

paths consisting of switched capacitors G, H, I, and J. It is seen later that, typically, no more than two of these capacitors are needed to realize the useful biquadratic transfer functions. Thus, most often it will be found that only seven capacitors are needed. Although the circuit schematic shown in Fig. la facilitates understanding the circuit, a more efficient implementation can be obtained by allowing similarly switched capacitors to share a common switch. Rearranging the circuit schematic in this way results in the minimum switch configuration shown in Fig. 1b. One can readily verify that the electrical behaviors of these circuits are identical.

To minimize[8,10] the deleterious effects of switch parasitics, we have avoided the use of toggle-switched capacitors[7] in which one end of the capacitor is permanently connected to ground. Furthermore, it is noted that the sc elements shown in Figs. 2a and 2b are equivalent in function. However, by discharging the capacitor C through ground, as per Fig. 2b (and the insert in Fig. 1), the parasitic switch capacitances are also discharged. For ideal operational amplifiers, the parasitic switch capacitances have absolutely no effect on the operation of the biquad. It is expected that the effect will only be negligibly enhanced[12] by the nonideal character of practical operational amplifiers.

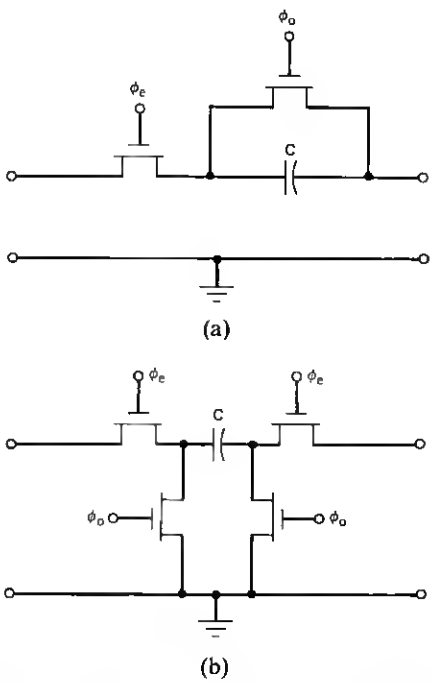


Fig. 2—Discharge type switched capacitors. (a) Typical realization. (b) Parasitic free realization.

The close analogy of SC filters to active-RC biquads has already been mentioned. In particular, note that the circuit with $E = 0$ is very similar in spirit to the three-operational amplifier multiple input biquad[13] except for the absence of the inverter, which is not needed for the SC filter. However, active-SC biquads offer even further versatility which to this point has not been exploited. Because of the inability to trim capacitors and the relative cost factors, practical active-RC biquads are constructed to be canonic in capacitors, namely, two. This constraint is unnecessarily placed on active-SC topologies when they are derived from an active-RC topology via a resistor-to-switched-capacitor replacement.[5-7,14] As we show, one can achieve interesting and beneficial results when this constraint is removed.

2.1 The transfer functions

Before deriving the transfer functions which characterize the general active-SC network of Fig. 1, it is necessary to consider the timing of the switches. Note that the schematics for some typical SC elements are shown as inserts in Fig. 1.

For simplicity in analysis, we assume the clocks ϕ_e and ϕ_o to be nonoverlapping with 50-percent duty cycle, as in Fig. 3. It is noted that switches clocked by ϕ_e close instantaneously at the $2k\tau$ (even) time instants and those clocked by ϕ_o close instantaneously at the $(2k + 1)\tau$ (odd) time instants. We also assume that the input signal is sampled and held over a full clock period, 2τ, as shown in Fig. 3. In fact, the switch phasings of the SC biquad have been chosen to operate with this kind of input. Under these conditions, we have

$$V_{\text{in}}^{o}(z) = z^{-1/2} V_{\text{in}}^{e}(z). \tag{3}$$

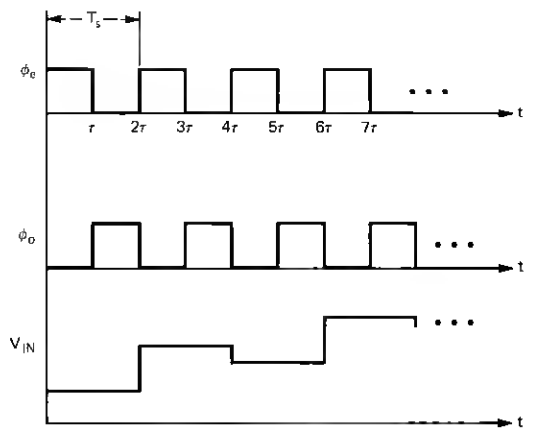


Fig. 3—Clock and input waveforms.

It follows then[16] that the output voltages appearing at the operational amplifier outputs are also held for the full clock period and change only at the even sampling instants:

$$V_{\text{out}}^{o}(z) = z^{-1/2} V_{\text{out}}^{e}(z). \tag{4}$$

This fact can also be surmised by inspection of Fig. 1a. Appendix A shows that the full-cycle S/H assumption can be relaxed. For the present, however, since both the input and the outputs are fully held, the even transfer functions provide all the information we need. For simplicity, therefore, the "even" superscript will be omitted from here on.

Let us now derive the voltage transfer functions T' and T for the networks of Fig. 1. As noted previously, these transfer functions are most conveniently expressed in the z-domain where $z = e^{sT_s}$ and $T_s = 2\tau$ represents a full clock period. Any SC network containing biphased switches can be conveniently transformed into a z-domain equivalent circuit.[15,16] With this equivalent circuit, one can then apply all the network tools available to continuous, linear, time-invariant networks. When the input signal is held over the full clock period, one can readily obtain[16] the equivalent circuit given in Fig. 4.

The desired transfer functions are then derived using straightforward nodal analysis:

$$T \triangleq \frac{V}{V_{\text{in}}}$$

$$= \frac{-Az^{-1}(G - Hz^{-1}) - D(1 - z^{-1})(I - Jz^{-1})}{Az^{-1}(C + E - Ez^{-1}) + D(1 - z^{-1})(F + B - Bz^{-1})} \tag{5a}$$

$$= -\frac{DI + (AG - DI - DJ)z^{-1} + (DJ - AH)z^{-2}}{D(F + B) + (AC + AE - DF - 2DB)z^{-1} + (DB - AE)z^{-2}}, \tag{5b}$$

and

$$T' \triangleq \frac{V'}{V_{\text{in}}}$$

$$= \frac{(I - Jz^{-1})(C + E - Ez^{-1}) - (G - Hz^{-1})(F + B - Bz^{-1})}{Az^{-1}(C + E - Ez^{-1}) + D(1 - z^{-1})(F + B - Bz^{-1})} \tag{6a}$$

$$= \frac{(IC + IE - GF - GB) + (FH + BH + BG - JC - JE - IE)z^{-1} + (EJ - BH)z^{-2}}{D(F + B) + (AC + AE - DF - 2DB)z^{-1} + (DB - AE)z^{-2}}. \tag{6b}$$

Before undertaking further analysis, some extraneous degrees of freedom will be eliminated. First, we arbitrarily set $A = B$. It may be shown that the net effect of this choice is to remove our ability to

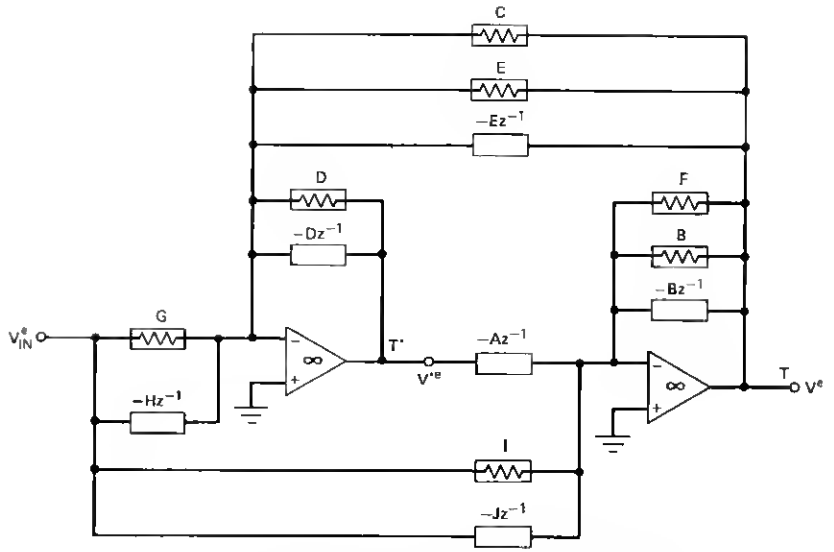


Fig. 4—z-domain equivalent circuit for the biquad in Fig. 1.

control the gain constants associated with T and T' simultaneously. Later we will show how, through scaling techniques, this degree of freedom can be restored to the circuit. Second, it is clear by examining the circuit of Fig. 1 that there is an arbitrary impedance scaling associated with each of the two stages. Thus, the two groups of capacitors (C, D, E, G, H) and (A, B, F, I, J) may each be arbitrarily and independently scaled without changing the transfer functions. Accordingly, we arbitrarily choose $B = 1$ and $D = 1$. This choice will also be ultimately overridden by minimum capacitor realization considerations.

In view of the above, we have

$$A = B = D = 1. \tag{7}$$

Substituting these into (5) and (6) yields the following simplified transfer functions:

$$T = -\frac{I + (G - I - J)z^{-1} + (J - H)z^{-2}}{(F + 1) + (C + E - F - 2)z^{-1} + (1 - E)z^{-2}} \tag{8}$$

and

$$T' = \frac{\begin{matrix}(IC + IE - FG - G)\\ + (FH + H + G - JC - JE - IE)z^{-1} + (EJ - H)z^{-2}\end{matrix}}{(F + 1) + (C + E - F - 2)z^{-1} + (1 - E)z^{-2}}. \tag{9}$$

Let us first examine the salient features of the transfer function T. Note that its poles are determined by C, E, and F, and its zeros by G,

H, I, and J. The fact that the poles and zeros are independently adjustable may prove to be useful in some filter or equalizer applications. It is also clear that the three numerator coefficients are independently adjustable thus permitting arbitrary zeros to be realized. The fact that any stable poles are also realizable will be demonstrated later.

Regarding the transfer function T', we first observe the obvious fact that its poles are identical to those of T. We note, however, that its zeros are formed in a more complicated fashion and they do not have the aforementioned independence property. Nevertheless, there are cases where T' provides a more economical realization of a given transfer function than T.

The zero-forming pairs (I, J) and (G, H) have some interesting alternate realizations. Using the techniques of Ref. 16, it may be shown that the pair I and J, for example, may be realized as shown in Fig. 5. Thus, one capacitor is eliminated not only when $I = 0$ or $J = 0$ but also when $I = J$. The equivalence of a pair of switched capacitors to one unswitched capacitor is quite fascinating in view of the switched-capacitor—resistance equivalence so commonly assumed in dealing with SC networks.

When $I = J$, not only is one capacitor eliminated, but sensitivity is usually improved since I and J now "track" perfectly. Even when $I \neq J$, the transformations may be useful to reduce sensitivity or to lower the total capacitance needed for a given case. For example, if $I = 13$ pf and $J = 12$ pf, transformation (a) can be applied, yielding new element values $I - J = 1$ pf and $J = 12$ pf. The transformation is obviously reversible; thus, the converse transformation can be applied to element pairs C,E and B,F. It should be noted that in arriving at these transformations we have assumed, as in Fig. 1, that terminals 1 and 2 are connected to a full clock period S/H voltage source and to a virtual ground, respectively. In Appendix A, we show that the full cycle S/H assumption can be conditionally relaxed.

Note that the SC elements in Fig. 5 all possess a z-domain admittance of the form $I - Jz^{-1}$. If the inverting switched capacitor J were replaced with a noninverting switched capacitor,[16] a z-domain admittance of the form $I + Jz^{-1}$ would be obtained. At times, it might be convenient from a synthesis point of view to have $I + Jz^{-1}$ admittances; however, as mentioned earlier, noninverting toggle-switched capacitors do introduce parasitics;[8,10] therefore, we avoid using this element. In spite of this omission, the circuit is capable of realizing all stable biquadratic transfer functions.

2.2 The E- and F-circuits

One final simplification we can make to the general biquad in Fig. 1 involves the elements E and F. As already mentioned, E and F are

Fig. 5—SC element transformations (ports 1 and 2 are assumed to be buffered).

redundant elements in the sense that they both provide damping. Consequently, they need not both be present in the same circuit. It is, therefore, convenient to define an "E-circuit" in which $E \neq 0$ and $F = 0$ and an "F-circuit" in which $F \neq 0$ and $E = 0$.

The transfer functions for these two circuits are

$$T'_E = \frac{I + (G - I - J)z^{-1} + (J - H)z^{-2}}{1 + (C + E - 2)z^{-1} + (1 - E)z^{-2}} \tag{10a}$$

$$T'_E = \frac{(IC + IE - G) + (H + G - JC - JE - IE)z^{-1} + (EJ - H)z^{-2}}{1 + (C + E - 2)z^{-1} + (1 - E)z^{-2}} \tag{10b}$$

and

$$T_F = -\frac{\hat{I} + (\hat{G} - \hat{I} - \hat{J})z^{-1} + (\hat{J} - \hat{H})z^{-2}}{(\hat{F} + 1) + (\hat{C} - \hat{F} - 2)z^{-1} + z^{-2}} \tag{11a}$$

$$T'_F = -\frac{(\hat{G}\hat{F} + \hat{G} - \hat{I}\hat{C}) + (\hat{J}\hat{C} - \hat{F}\hat{H} - \hat{H} - \hat{G})z^{-1} + \hat{H}z^{-2}}{(\hat{F} + 1) + (\hat{C} - \hat{F} - 2)z^{-1} + z^{-2}}. \tag{11b}$$

The "hats" are placed on the F-circuit elements in order to distinguish them from the E-circuit elements.

Let us briefly examine these transfer functions. Note that the numerators of T_E and T_F are identical, while the numerators of T'_E and T'_F are quite different. Thus for a given design in which the desired output is V, the T' as well as the unscaled dynamic range of V' may be quite different for the two networks. The analogous situation is obtained if the desired output is V'. These differences will ultimately affect the final scaled capacitor values and the total capacitance required to realize the circuit. Significant sensitivity differences between the four possible realizations of a given transfer function may also exist. These points will be illustrated via examples in Section IV.

2.4 Sensitivities

The sensitivities for the E- and F-circuits are at least comparable to any active-RC biquad. One can arrive at this conclusion by examining the Q and ω_o relations and associated sensitivities for a moderate-to-high-Q resonant response.

For any pair of complex conjugate poles in the z-domain, one can write the denominator as:

$$D(z) = 1 + \alpha z^{-1} + \beta z^{-2} \tag{12a}$$

$$= (1 - re^{j\theta}z^{-1})(1 - re^{-j\theta}z^{-1})$$

$$= 1 - 2r\cos\theta z^{-1} + r^2 z^{-2}. \tag{12b}$$

By analogy to the continuous case, the following equations involving

the resonant frequency ω_o and Q can be written:

$$\theta \approx 2\pi \frac{\omega_o}{\omega_s} = \omega_o T_s \tag{13}$$

and (14)

$$\frac{1}{2Q} \approx \frac{1-r}{\theta} = \frac{1-r}{\omega_o T_s},$$

which implies

$$r \approx 1 - \frac{\omega_o T_s}{2Q}. \tag{15}$$

Therefore, it follows from (12) through (15) that

$$\alpha \approx -2\left(1 - \frac{\omega_o T_s}{2Q}\right)\cos \omega_o T_s \tag{16a}$$

$$\beta \approx \left(1 - \frac{\omega_o T_s}{2Q}\right)^2. \tag{16b}$$

Whenever $\omega_o T_s \ll 1$, i.e., the sampling rate is high and $Q \gg 1$, the above expressions may be further approximated:

$$\alpha \approx -2\left(1 - \frac{\omega_o T_s}{2Q}\right)\left(1 - \frac{\omega_o^2 T_s^2}{2}\right)$$

$$\approx -2 + \frac{\omega_o T_s}{Q} + \omega_o^2 T_s^2 \tag{17a}$$

and

$$\beta \approx 1 - \frac{\omega_o T_s}{Q}. \tag{17b}$$

Consider first the E-circuit. After suitable manipulations, the denominator of (5) becomes (with $F = 0$)

$$D_E(z) = 1 + \left(-2 + \frac{AC}{DB} + \frac{AE}{DB}\right)z^{-1} + \left(1 - \frac{AE}{DB}\right)z^{-2}. \tag{18}$$

Comparing this with (12a) and (17) immediately yields

$$\frac{\omega_o T_s}{Q} \approx \frac{AE}{DB} \tag{19a}$$

and

$$\omega_o^2 T_s^2 \approx \frac{AC}{DB}. \tag{19b}$$

Therefore,

$$\omega_o T_s \approx \left(\frac{AC}{DB}\right)^{1/2} \tag{20a}$$

and

$$Q \approx \frac{1}{E}\left(\frac{DBC}{A}\right)^{1/2}. \tag{20b}$$

Similarly, it may be shown that, for the F-circuit,

$$\omega_o T_s \approx \left(\frac{\hat{A}\hat{C}}{\hat{D}\hat{B} + \hat{D}\hat{F}}\right)^{1/2} \tag{21a}$$

and

$$Q \approx \left[\frac{\hat{A}\hat{C}}{\hat{D}\hat{F}}\left(1 + \frac{\hat{B}}{\hat{F}}\right)\right]^{1/2}. \tag{21b}$$

From (20) and (21), it is seen that ω_o and Q are controlled by the ratios of four or five capacitors. Furthermore, it is clear that

$$|S_x^{\omega_o}| \leq \tfrac{1}{2} \quad \text{and} \quad |S_x^Q| \leq 1, \tag{22}$$

where x denotes any capacitor in the E- or F-circuits. This situation compares favorably to the active-RC case,[1,2,17] where a minimum of four passive elements, namely, two RC products, determines ω_o. Since, in practice, ratios of capacitors can be more tightly controlled than individual resistors and capacitors, the active-SC realization can be expected to be superior to the active-RC case with respect to initial (untuned) response as well as temperature and aging variations.*

Even though, in practice, the ω_o variation is usually the most significant contributor to the overall variation in the response,[17] we note that the Q sensitivity of the active-SC circuit is also low.

The overall circuit sensitivity is also affected, of course, by the contribution of the numerator. This aspect of the problem is not amenable to a general analysis and has to be handled on a case-by-case basis. It has been our experience that T designs provide lower sensitivity realizations than T' designs. It can be seen from (5) and (6) that the numerator of T is simpler than the numerator of T'. Although one might expect the pole-zero tracking afforded by the T' designs to yield lower sensitivities for some applications, we find that, because of the cancellations which occur in the coefficients, larger sensitivities are often incurred.

* Since T_s is normally derived from a very stable clock, it is assumed to be invariant.

III. SYNTHESIS

The synthesis of the biquad begins with the identification of the desired transfer function. This determination ultimately depends upon the frequency domain specifications which can then be transformed in some manner to a z-domain transfer function. The individual biquad transfer functions are then obtained by factoring this higher order z-domain transfer function.

Once the desired biquadratic transfer function is identified, the unscaled capacitor values are determined from (10) or (11) for the E- or F-circuit, respectively. Once this basic design is obtained, the final step consists of scaling the capacitors to adjust the dynamic range at the output of the other operational amplifier. It is then convenient to rescale the admittances in each of the two stages to obtain a minimum capacitance value of 1 unit in each stage. The actual minimum value of capacitance which can be realized depends on the technology, the desired precision of the transfer function, and the estimated effects of parasitics. A minimum capacitance of 1 pf will be used in this paper.

3.1 z-domain biquadratic transfer functions

Like digital filters, switched-capacitor filters are most conveniently synthesized from a z-domain transfer function. Several methods are available[11] for obtaining a z-domain transfer function from frequency domain specifications. Perhaps the most useful of these is based on the bilinear transformation[11] which can be shown to preserve "maximally flat" or "equal ripple" properties. This method starts with a suitably prewarped analog transfer function in the s-domain. This analog transfer function is then converted to a z-domain transfer function using the bilinear transformation,

$$s = \frac{2}{T_s}\frac{1 - z^{-1}}{1 + z^{-1}}, \tag{23}$$

where, it is recalled, T_s denotes the full clock period. The application of the bilinear transform to an analog biquadratic transfer function yields a z-domain transfer function which is also biquadratic. Of consequence to the ultimate form of low-pass and bandpass transfer functions is the fact that analog zeros at $s = \infty$ map into finite z-domain zeros at $z = -1$. Other transformations,[8] such as

$$s = \frac{1}{T_s}\frac{1 - z^{-1}}{z^{-1}}, \tag{24}$$

do not have this mapping property. Using (24), the mapping of the poles is also somewhat different than that obtained via the bilinear transformation.

3.2 Pole placement

At this point, it is appropriate to consider the stability and realizability of the proposed circuits. It is, of course, desirable to be able to realize all stable pole positions. Stability for a biquad can be conveniently expressed[18] in the α, β parameter space as the area within the shaded triangle shown in Fig. 6. The upper parabolic area of the triangle represents the α, β values for stable, complex poles. The remainder of the upper triangular area, where $\beta > 0$, corresponds to real pole pairs which lie pairwise to the left or right of $z = 0$, while the lower triangular area, where $\beta < 0$, corresponds to real poles which lie on alternate sides of $z = 0$. Clearly, the upper portion of the triangle, i.e., $\beta > 0$, represents most of the useful pole locations for frequency selective filters.

Consider first the E-circuit realizability properties. Comparing (2) and (10) yields

$$\alpha = E + C - 2 \tag{25a}$$

$$\beta = 1 - E \tag{25b}$$

and, therefore,

$$\alpha + \beta = C - 1. \tag{25c}$$

Since $E \geq 0$ and $C \geq 0$, we immediately have from (25a) and (25c):

$$\alpha \geq -2 \tag{26a}$$

$$\beta \leq 1 \tag{26b}$$

$$\alpha + \beta \geq -1. \tag{26c}$$

Thus, the α, β values realizable with the E-circuit are confined within the wedge-like area shown in Fig. 7a. This area includes all the stable

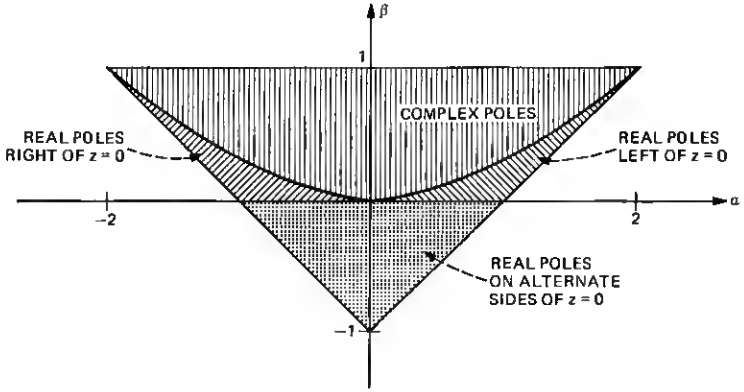
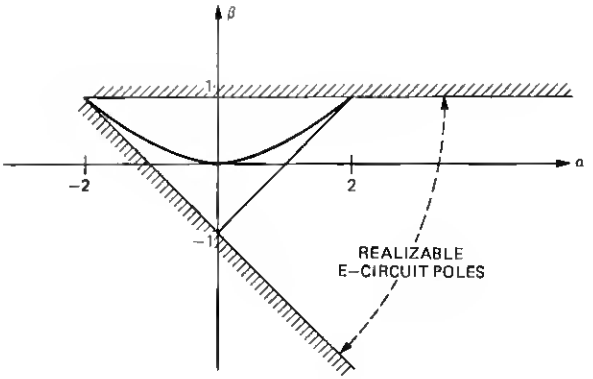
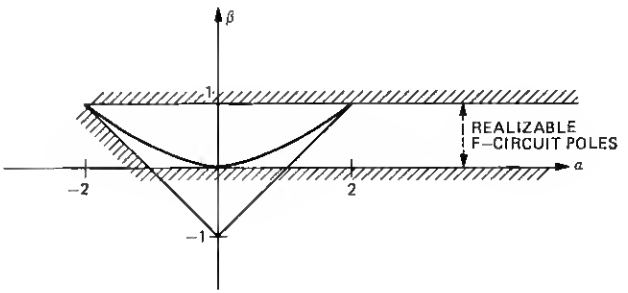


Fig. 6—Triangle of stable pole positions for $D(z) = 1 + \alpha z^{-1} + \beta z^{-2}$.



(a)



(b)

Fig. 7—Pole placement realizability conditions for (a) *E*-circuit and (b) *F*-circuit.

region as well as a portion of the remaining unstable area. *E*-circuits which are unstable must possess real poles.

The *F*-circuit realizability conditions can be derived similarly from (11):

$$0 \leq \beta \leq 1 \tag{27a}$$

and

$$\alpha + \beta \geq -1. \tag{27b}$$

These equations define the semiwedge-like area shown in Fig. 7b. Although this area is more restricted than that representing realizable *E*-circuit poles, the *F*-circuit is seen to be able to realize all the useful stable pole positions. The only stable case not realizable with the *F*-circuit has two real poles of opposite signs. Also, unstable *F*-circuits must have real poles of the same sign.

Now that we have established the realizability conditions for the *E*-

and F-circuits, let us state the pole placement synthesis equations in terms of the z-domain transfer function coefficients α and β. For the E-circuit, the synthesis equations can be stated as

$$E = 1 - \beta \tag{28a}$$

and

$$C = 1 + \beta + \alpha. \tag{28b}$$

Similarly, for the F-circuit we have

$$\hat{F} = \frac{1 - \beta}{\beta} \tag{29a}$$

and

$$\hat{C} = \frac{1 + \alpha + \beta}{\beta}. \tag{29b}$$

Equations (28) and (29) yield nonnegative values for E, C and $\hat{F}$, $\hat{C}$ within the realizability areas sketched in Figs. 7a and 7b, respectively. Also note that $\hat{F}$ and $\hat{C}$ for the F-circuit can be obtained from values calculated for E and C for the E-circuit using the simple relations

$$\hat{F} = \frac{E}{1 - E} \tag{30a}$$

and

$$\hat{C} = \frac{C}{1 - E}. \tag{30b}$$

As noted previously, it is often convenient to derive the z-domain transfer function from the prewarped analog requirements via the bilinear transformation given by (23). Once an appropriate prewarped s-domain transfer function has been determined, one can then derive simple synthesis relations for the pole-determining capacitors in terms of its coefficients. Let the denominator of the prewarped s-domain transfer function be

$$D(s) = s^2 + as + b. \tag{31}$$

Then, substituting for s the bilinear transformation of (23) and equating the coefficients of the resulting z-domain quadratic polynomial with those of the denominator of T_E (or T'_E) yields

$$E = \frac{aT_s}{1 + \frac{aT_s}{2} + b\frac{T_s^2}{4}} \tag{32a}$$

and

$$C = \frac{bT_s^2}{1 + \dfrac{aT_s}{2} + b\dfrac{T_s^2}{4}}. \tag{32b}$$

Similar expressions for the F-circuit may be written

$$\hat{F} = \frac{aT_s}{1 - \dfrac{aT_s}{2} + \dfrac{bT_s^2}{4}} \tag{33a}$$

and

$$\hat{C} = \frac{bT_s^2}{1 - \dfrac{aT_s}{2} + \dfrac{bT_s^2}{4}}. \tag{33b}$$

In summary, when the desired z-domain biquadratic transfer function is known, capacitor values E, C or $\hat{F}$, $\hat{C}$ are readily evaluated according to (28) or (29), respectively. Alternatively, when an appropriately prewarped transfer function is known, the capacitor values E, C or $\hat{F}$, $\hat{C}$ can be evaluated in terms of the coefficients of the prewarped analog function and the sampling period T_s according to (32) or (33), respectively.

3.3 Zero placement

Before deriving the synthesis relations for the zeros, it is instructive to list the z-domain transfer functions for the well-known generic forms; namely, low-pass (LP), high-pass (HP), bandpass (BP), low-pass notch (LPN), high-pass notch (HPN), and all-pass (AP).[19] The numerators, with reference to (2), for these generic forms are listed in Table I. The LP and BP functions are particularly interesting in that there are several different forms which can be used. These forms are referred to in Table I as LP_{ij} and BP_{ij}, where i denotes the number of $1 + z^{-1}$ factors and j the number of z^{-1} factors. As already noted, the zeros at $z = -1$ arise only when the bilinear transform is used. These transfer functions, of course, exhibit steeper cutoff in the vicinity of half the sampling rate, but they may not afford the most economical realization. As a rule of thumb, the additional cutoff will become less and less important as the sampling frequency increases with respect to the pole-zero locations, i.e., as $\omega_0 T_s \rightarrow$ small.

The number of z^{-1}, i.e., delay, terms will usually be immaterial. In these cases, economy of realization or perhaps sensitivity considerations might indicate the best choice. Note, however, that if there is additional feedback around any biquad block, the delay term becomes critical.

Table I—Generic biquadratic transfer functions

Generic Form	Numerator $N(z)$
LP 20 (bilinear transform)	$K(1+z^{-1})^2$
LP 11	$Kz^{-1}(1+z^{-1})$
LP 10	$K(1+z^{-1})$
LP 02	Kz^{-2}
LP 01	Kz^{-1}
LP 00	K
BP 10 (bilinear transform)	$K(1-z^{-1})(1+z^{-1})$
BP 01	$Kz^{-1}(1-z^{-1})$
BP 00	$K(1-z^{-1})$
HP	$K(1-z^{-1})^2$
LPN	$K(1+\epsilon z^{-1}+z^{-2}),\ \epsilon > \alpha/\sqrt{\beta},\ \beta > 0$
HPN	$K(1+\epsilon z^{-1}+z^{-2}),\ \epsilon < \alpha/\sqrt{\beta},\ \beta > 0$
AP	$K(\beta+\alpha z^{-1}+z^{-2})$
General	$\gamma+\epsilon z^{-1}+\delta z^{-2}$

As already noted in connection with (10) and (11), T_E and T_F have identical numerators except for the $1/(1+\hat{F})$ gain constant term. For convenience, the numerator of T_E is repeated below:

$$N(z) = -I + (G - I - J)z^{-1} + (J - H)z^{-2}. \tag{34}$$

It is evident that there are enough degrees of freedom here to choose the three coefficients independently and thus realize arbitrary zero locations; the fact that the leading coefficient is nonpositive is a trivial constraint. In Table II a complete set of design equations is given for the special generic transfer functions of Table I as well as for the general case. For each of the cases, a "simple" solution is also listed. These simple solutions, which are not unique, lead to fewer number of capacitors by setting as many of the capacitors G, H, I, and J as possible to zero, or by having $G = H$ or $I = J$ which, according to Fig. 5, also eliminates a capacitor as well as some switches.

It should be noted that the F-circuit capacitors $\hat{G}$, $\hat{H}$, $\hat{I}$, and $\hat{J}$ are related to G, H, I, and J by

$$\hat{x} = (1 + \hat{F})x \quad \text{where} \quad x = G, H, I, J. \tag{35}$$

For this reason a separate table need not be given for the synthesis of the zeros of T_F.

Similar zero-placement synthesis conditions are listed for transfer functions T'_E and T'_F in Tables III and IV, respectively. It is noted that these synthesis equations require prior knowledge of either E, C or $\hat{F}$, $\hat{C}$, in contrast to the T_E or T_F case.

This completes the material on zero-placement. It will be recognized that, for any given transfer function, four alternative realizations exist, i.e., T_E, T'_E, T_F, and T'_F. In the case of LP or BP designs, additional degrees of freedom exist, as there may be a choice of transfer functions (see Table I). At this point, we cannot state any general rule for

Table II—Zero placement formulas for T_E and T_F

Filter Type	Design Equations	Simple Solution
LP 20	$I = \|K\|$ $G - I - J = 2\|K\|$ $J - H = \|K\|$	$I = J = \|K\|$ $G = 4\|K\|, \quad H = 0$
LP 11	$I = 0$ $G - I - J = \pm\|K\|$ $J - H = \pm\|K\|$	$I = 0, \quad J = \|K\|$ $G = 2\|K\|, \quad H = 0$
LP 10	$I = \|K\|$ $G - I - J = \|K\|$ $J - H = 0$	$I = \|K\|, \quad J = 0$ $G = 2\|K\|, \quad H = 0$
LP 02	$I = 0$ $G - I - J = 0$ $J - H = \pm\|K\|$	$I = J = 0$ $G = 0, \quad H = \|K\|$
LP 01	$I = 0$ $G - I - J = \pm\|K\|$ $J - H = 0$	$I = J = 0$ $G = \|K\|, \quad H = 0$
LP 00	$I = \|K\|$ $G - I - J = 0$ $J - H = 0$	$I = \|K\|, \quad J = 0$ $G = \|K\|, \quad H = 0$
BP 10	$I = \|K\|$ $G - I - J = 0$ $J - H = -\|K\|$	$I = \|K\|, \quad J = 0$ $G = H = \|K\|$
BP 01	$I = 0$ $G - I - J = \pm\|K\|$ $J - H = \mp\|K\|$	$I = 0, \quad J = \|K\|$ $G = H = 0$
BP 00	$I = \|K\|$ $G - I - J = -\|K\|$ $J - H = 0$	$I = \|K\|, \quad J = 0$ $G = H = 0$
HP	$I = \|K\|$ $G - I - J = -2\|K\|$ $J - H = \|K\|$	$I = J = \|K\|$ $G = H = 0$
HPN and LPN	$I = \|K\|$ $G - I - J = \|K\|\epsilon$ $J - H = \|K\|$	$I = J = \|K\|$ $G = \|K\|\{2 + \epsilon\}, \quad H = 0$
AP ($\beta > 0$)	$I = \|K\|\beta$ $G - I - J = \|K\|\alpha$ $J - H = \|K\|$	$I = \|K\|\beta, \quad J = \|K\|$ $G = \|K\|(1 + \beta + \alpha) = \|K\|C$ $H = 0$
General ($\gamma > 0$)	$I = \gamma$ $G - I - J = \epsilon$ $J - H = \delta$	$I = \gamma$ $J = \delta + x$ $G = \gamma + \delta + \epsilon + x$ $H = x \geq 0$

Note: $\hat{G} = G(1 + \hat{F})$, $\hat{H} = H(1 + \hat{F})$, $\hat{I} = I(1 + \hat{F})$, and $\hat{J} = J(1 + \hat{F})$.

Table III—Zero placement formulas for T_E'

Filter Type	Design Equations	Simple Solution
LP 20	$IC + IE - G = \pm\lvert K\rvert$ $H + G - JC - JE - IE = \pm 2\lvert K\rvert$ $EJ - H = \pm\lvert K\rvert$	$I = \frac{\lvert K\rvert(4E + C)}{EC}, \quad J = \frac{\lvert K\rvert}{E}$ $G = \frac{\lvert K\rvert(2E + C)^2}{EC}, \quad H = 0$
LP 11	$IC + IE - G = 0$ $H + G - JC - JE - IE = \pm\lvert K\rvert$ $EJ - H = \pm\lvert K\rvert$	$I = \frac{\lvert K\rvert(2E + C)}{EC}, \quad J = \frac{\lvert K\rvert}{E}$ $G = \frac{\lvert K\rvert(E + C)(2E + C)}{EC}, \quad H = 0$
LP 10	$IC + IE - G = \pm\lvert K\rvert$ $H + G - JC - JE - IE = \pm\lvert K\rvert$ $EJ - H = 0$	$I = \frac{2\lvert K\rvert}{C}, \quad J = 0$ $G = \frac{\lvert K\rvert(E + C)^2}{EC}, \quad H = 0$
LP 02	$IC + IE - G = 0$ $H + G - JC - JE - IE = 0$ $EJ - H = \pm\lvert K\rvert$	$I = \frac{\lvert K\rvert(E + C)}{EC}, \quad J = \frac{\lvert K\rvert}{E}$ $G = \frac{\lvert K\rvert(E + C)^2}{EC}, \quad H = 0$
LP 01	$IC + IE - G = 0$ $H + G - JC - JE - IE = \pm\lvert K\rvert$ $EJ - H = 0$	$I = \frac{\lvert K\rvert}{C}, \quad J = 0$ $G = \frac{\lvert K\rvert(E + C)}{C}, \quad H = 0$
LP 00	$IC + IE - G = \pm\lvert K\rvert$ $H + G - JC - JE - IE = 0$ $EJ - H = 0$	$I = \frac{\lvert K\rvert}{C}, \quad J = 0$ $G = \frac{\lvert K\rvert E}{C}, \quad H = 0$
BP 10	$IC + IE - G = \pm\lvert K\rvert$ $H + G - JC - JE - IE = 0$ $EJ - H = \mp\lvert K\rvert$	$I = J = \frac{\lvert K\rvert}{E}$ $G = \frac{\lvert K\rvert(2E + C)}{E}, \quad H = 0$
BP 01	$IC + IE - G = 0$ $H + G - JC - JE - IE = \pm\lvert K\rvert$ $EJ - H = \mp\lvert K\rvert$	$I = J = 0$ $G = 0, \quad H = \lvert K\rvert$
BP 00	$IC + IE - G = \pm\lvert K\rvert$ $H + G - JC - JE - IE = \mp\lvert K\rvert$ $EJ - H = 0$	$I = 0, \quad J = 0$ $G = \lvert K\rvert, \quad H = 0$
HP	$IC + IE - G = \pm\lvert K\rvert$ $H + G - JC - JE - IE = \mp 2\lvert K\rvert$ $EJ - H = \pm\lvert K\rvert$	$I = J = 0$ $G = H = \lvert K\rvert$
HPN and LPN	$IC + IE - G = \pm\lvert K\rvert$ $H + G - JC - JE - IE = \pm\lvert K\rvert\epsilon$ $EJ - H = \pm\lvert K\rvert$	See general solution below
AP	$IC + IE - G = \pm\lvert K\rvert\beta$ $H + G - JC - JE - IE = \pm\lvert K\rvert\alpha$ $EJ - H = \pm\lvert K\rvert$	See general solution below

Table III—*Continued*

Filter Type	Design Equations	Simple Solution
General	$IC + IE - G = \gamma$	$I = \frac{\gamma + \delta + \epsilon}{C} + \frac{\delta}{E}, \quad J = \frac{\delta}{E}$
$\delta > 0$	$H + G - JC - JE - IE = \epsilon$ $EJ - H = \delta$	$G = I(C + E) - \gamma \quad H = 0$

selecting the optimum transfer function from these four functions. We can show for specific designs that considerable differences in total capacitance and sensitivity can be obtained for equivalent T_E, T_F, T'_E, and T'_F designs.

Hopefully, as we gain more experience in active-sc design, some insights will be acquired to shorten the design procedure. In the meanwhile, enough alternatives have to be tried until a satisfactory solution is obtained.

3.4 Capacitor value scaling

The synthesis equations given in the previous subsections result in unscaled capacitor values. To complete the synthesis, some scaling is required. The first order of business is to adjust the voltage level at the "secondary" output. If this voltage is too high, overloads will result, while if it is too low, unnecessary noise penalties may be taken.

Although the voltage levels may be obtained using analysis techniques,[16] the simplest procedure is to simulate the unscaled circuit[20] on a program such as CAPECOD.[21] This also serves as a confirmation of the correctness of the design.

To adjust the voltage level V', i.e., the flat gain of T', without affecting T, only the capacitors A and D need be scaled. More precisely, if it is desired to modify the gain constant associated with V' according to

$$T' \rightarrow \mu T', \tag{36}$$

then it is only necessary to scale A and D as

$$(A, D) \rightarrow \left(\frac{1}{\mu} A, \frac{1}{\mu} D\right). \tag{37}$$

The gain constant associated with T remains invariant under this scaling. The correctness of this procedure follows directly from simple signal flow graph concepts. Note that A and D are the only two capacitors connected to the operational amplifier output node.

In a similar fashion, it can be shown that, if the flat gain associated with V is to be modified, i.e.,

Table IV—Zero placement formulas for T_F'

Filter Type	Design Equations	Simple Solution
LP 20	$\hat{G}\hat{F} + \hat{G} - \hat{I}\hat{C} = \lvert K\rvert(1+\hat{F})$ $\hat{J}\hat{C} - \hat{F}\hat{H} - \hat{H} - \hat{G} = 2\lvert K\rvert(1+\hat{F})$ $\hat{H} = \lvert K\rvert(1+\hat{F})$	$\hat{I} = 0, \quad \hat{J} = \dfrac{\lvert K\rvert(2+\hat{F})^2}{\hat{C}}$ $\hat{G} = \lvert K\rvert, \quad \hat{H} = \lvert K\rvert(1+\hat{F})$
LP 11	$\hat{G}\hat{F} + \hat{G} - \hat{I}\hat{C} = 0$ $\hat{J}\hat{C} - \hat{F}\hat{H} - \hat{H} - \hat{G} = \lvert K\rvert(1+\hat{F})$ $\hat{H} = \lvert K\rvert(1+\hat{F})$	$\hat{I} = 0, \quad \hat{J} = \dfrac{\lvert K\rvert(1+\hat{F})(2+\hat{F})}{\hat{C}}$ $\hat{G} = 0, \quad \hat{H} = \lvert K\rvert(1+\hat{F})$
LP 10	$\hat{G}\hat{F} + \hat{G} - \hat{I}\hat{C} = \pm\lvert K\rvert(1+\hat{F})$ $\hat{J}\hat{C} - \hat{F}\hat{H} - \hat{H} - \hat{G} = \pm\lvert K\rvert(1+\hat{F})$ $\hat{H} = 0$	$\hat{I} = 0, \quad \hat{J} = \dfrac{\lvert K\rvert(2+\hat{F})}{\hat{C}}$ $\hat{G} = \lvert K\rvert, \quad \hat{H} = 0$
LP 02	$\hat{G}\hat{F} + \hat{G} - \hat{I}\hat{C} = 0$ $\hat{J}\hat{C} - \hat{F}\hat{H} - \hat{H} - \hat{G} = 0$ $\hat{H} = \lvert K\rvert(1+\hat{F})$	$\hat{I} = 0, \quad \hat{J} = \dfrac{\lvert K\rvert(1+\hat{F})^2}{\hat{C}}$ $\hat{G} = 0, \quad \hat{H} = \lvert K\rvert(1+\hat{F})$
LP 01	$\hat{G}\hat{F} + \hat{G} - \hat{I}\hat{C} = 0$ $\hat{J}\hat{C} - \hat{F}\hat{H} - \hat{H} - \hat{G} = \pm K(1+\hat{F})$ $\hat{H} = 0$	$\hat{I} = 0, \quad \hat{J} = \dfrac{\lvert K\rvert(1+\hat{F})}{\hat{C}}$ $\hat{G} = 0, \quad \hat{H} = 0$
LP 00	$\hat{G}\hat{F} + \hat{G} - \hat{I}\hat{C} = \pm\lvert K\rvert(1+\hat{F})$ $\hat{J}\hat{C} - \hat{F}\hat{H} - \hat{H} - \hat{G} = 0$ $\hat{H} = 0$	$\hat{I} = \dfrac{\lvert K\rvert(1+\hat{F})}{\hat{C}}, \quad \hat{J} = 0$ $\hat{G} = 0, \quad \hat{H} = 0$
BP 10	$\hat{G}\hat{F} + \hat{G} - \hat{I}\hat{C} = -\lvert K\rvert(1+\hat{F})$ $\hat{J}\hat{C} - \hat{F}\hat{H} - \hat{H} - \hat{G} = 0$ $\hat{H} = \lvert K\rvert(1+\hat{F})$	$\hat{I} = \dfrac{\lvert K\rvert(1+\hat{F})}{\hat{C}}, \quad \hat{J} = \dfrac{\lvert K\rvert(1+\hat{F})^2}{\hat{C}}$ $\hat{G} = 0, \quad \hat{H} = \lvert K\rvert(1+\hat{F})$
BP 01	$\hat{G}\hat{F} + \hat{G} - \hat{I}\hat{C} = 0$ $\hat{J}\hat{C} - \hat{F}\hat{H} - \hat{H} - \hat{G} = -\lvert K\rvert(1+\hat{F})$ $\hat{H} = \lvert K\rvert(1+\hat{F})$	$\hat{I} = 0, \quad \hat{J} = \dfrac{\lvert K\rvert\hat{F}(1+\hat{F})}{\hat{C}}$ $\hat{G} = 0, \quad \hat{H} = \lvert K\rvert(1+\hat{F})$
BP 00	$\hat{G}\hat{F} + \hat{G} - \hat{I}\hat{C} = \pm\lvert K\rvert(1+\hat{F})$ $\hat{J}\hat{C} - \hat{F}\hat{H} - \hat{H} - \hat{G} = \mp\lvert K\rvert(1+\hat{F})$ $\hat{H} = 0$	$\hat{I} = \hat{J} = \dfrac{\lvert K\rvert(1+\hat{F})}{\hat{C}}$ $\hat{G} = \hat{H} = 0$
HP	$\hat{G}\hat{F} + \hat{G} - \hat{I}\hat{C} = \lvert K\rvert(1+\hat{F})$ $\hat{J}\hat{C} - \hat{F}\hat{H} - \hat{H} - \hat{G} = -2\lvert K\rvert(1+\hat{F})$ $\hat{H} = \lvert K\rvert(1+\hat{F})$	$\hat{I} = 0, \quad \hat{J} = \dfrac{\lvert K\rvert\hat{F}^2}{\hat{C}}$ $\hat{G} = \lvert K\rvert, \quad \hat{H} = \lvert K\rvert(1+\hat{F})$
HPN and LPN	$\hat{G}\hat{F} + \hat{G} - \hat{I}\hat{C} = \lvert K\rvert(1+\hat{F})$ $\hat{J}\hat{C} - \hat{F}\hat{H} - \hat{H} - \hat{G} = -\lvert K\rvert\epsilon(1+\hat{F})$ $\hat{H} = \lvert K\rvert(1+\hat{F})$	See general solution below
AP	$\hat{G}\hat{F} + \hat{G} - \hat{I}\hat{C} = \lvert K\rvert\beta(1+\hat{F})$ $\hat{J}\hat{C} - \hat{F}\hat{H} - \hat{H} - \hat{G} = \lvert K\rvert\alpha(1+\hat{F})$ $\hat{H} = \lvert K\rvert(1+\hat{F})$	See general solution below
General	$\hat{G}\hat{F} + \hat{G} - \hat{I}\hat{C} = \gamma(1+\hat{F})$	$I = x \geq 0$

Table IV—*Continued*

Filter Type	Design Equations	Simple Solution
$\delta > 0$	$\hat{J}\hat{C} - \hat{F}\hat{H} - \hat{H} - \hat{G} = \epsilon(1 + \hat{F})$	$\hat{J} = \dfrac{\delta(1 + \hat{F})^2 + \epsilon(1 + \hat{F}) + \gamma}{\hat{C}} + \dfrac{x}{1 + \hat{F}}$
	$\hat{H} = \delta(1 + \hat{F})$	$\hat{G} = \gamma + \dfrac{\hat{C}}{1 + \hat{F}} x$ $\hat{H} = \delta(1 + \hat{F})$

$$T \rightarrow \nu T, \tag{38}$$

the following capacitors must be scaled:

$$(B, C, E, F) \rightarrow \left(\frac{1}{\nu} B, \frac{1}{\nu} C, \frac{1}{\nu} E, \frac{1}{\nu} F\right) \tag{39}$$

Once satisfactory gain levels have been obtained at both outputs, it is convenient to scale the admittances associated with each stage so that the minimum capacitance value in the circuit becomes unity. This makes it easier to observe the maximum capacitance ratios required to realize a given circuit and also serves to "standardize" different designs so that the total capacitance required can be readily observed. The two groups of capacitors which are to be scaled together are listed below.

Group 1: (C, D, E, G, H).

Group 2: (A, B, F, I, J).

Note that capacitors in each group are distinguished by the fact that they are all incident on the same input node of one of the operational amplifiers.

This completes the design process for synthesizing practical sc-biquad networks. In the next section, a detailed example is given to demonstrate each step of the design.

IV. DESIGN EXAMPLES

In this section, some illustrative examples will be given. The first example is a low-pass notch network whose design is followed through, step by step, to illustrate the design procedure. The second example is a bandpass. For this case, eight different designs are displayed to demonstrate the versatility of the active-sc topologies and to provide some insight into the relative merits of different realizations.

4.1 Low-pass notch circuit

The transfer function to be realized will be based on the s-domain transfer function shown below:

$$T(s) = \frac{0.891975s^2 + (1.140926 \times 10^8)}{s^2 + 356.047s + (1.140926 \times 10^8)}. \tag{40}$$

This transfer function provides a notch frequency of $f_z = 1800$ Hz, a peak corresponding to a quality factor $Q_p = 30$ at $f_p = 1700$ Hz and 0 dB dc gain. The assigned sampling frequency is 128 kHz, i.e., $T_s = 7.8125$ μs.

The z-domain transfer function is conveniently obtained via the bilinear transformation shown in (23). Because the band-edge frequency of 1700 Hz is much less than the sampling rate, it is not necessary to prewarp the $T(s)$ given in (40). Applying the bilinear transformation to (40) yields, after some algebraic manipulations:

$$T(z) = 0.89093 \frac{1 - 1.99220z^{-1} + z^{-2}}{1 - 1.99029z^{-1} + 0.99723z^{-2}}. \tag{41}$$

Note that in obtaining this transfer function a high degree of numerical precision is required. However, this does not result in high sensitivities, since the capacitor ratios define only the departures from -2 and $+1$ in the above terms.

Only the T_E and T_F realizations of the above circuit will be given here, as these circuits are more economical in the number of capacitors required for realization. The synthesis itself is straightforward. The capacitors C, E or $\hat{C}$, $\hat{F}$ are determined from (28) or (29), respectively, while the capacitors G, H, I, J, or $\hat{G}$, $\hat{H}$, $\hat{I}$, $\hat{J}$ are obtained from the "simple solution" entry in Table II. Finally, of course, A, B, D or $\hat{A}$, $\hat{B}$, $\hat{D}$ are set equal to unity according to (7). The resulting unscaled capacitor values are given in the appropriate columns of Table V. Note that, in this table and all succeeding ones, the hats are omitted from the F-circuit capacitors for notational convenience. Also note that since $I = J$ these two switched capacitors are replaced by the unswitched capacitor K, $(K = I = J)$, in accordance with Fig. 5.

At this point, the unscaled E- and F-circuits were simulated via CAPECOD.[20,21] These results confirmed that the T_E and T_F were both correct. In particular, the maximum gain in both these realizations was approximately 10.56 dB. However, the maximum gains for T'_E and T'_F were very low. It was decided to increase these gains also to a maximum of 10.56 dB. In this way, the first stage is no more susceptible to overloads than the second stage. Specifically, it was found that

$$T'_{E\,\mathrm{MAX}} \approx -11.05 \text{ dB}, \qquad T'_{F\,\mathrm{MAX}} \approx -10.96 \text{ dB}. \tag{42}$$

Therefore, in accordance with (36),

$$\mu = 12.0365, \qquad \hat{\mu} = 11.9124. \tag{43}$$

Using these factors to rescale A, D and $\hat{A}$, $\hat{D}$, respectively, as given in (37), yields the "dynamic range adjusted" capacitor values shown in Table V. Finally, the capacitors associated with each operational amplifier stage are separately rescaled so that the minimum capacitance value becomes 1 pF. These "final" values are also shown in Table V.

In comparing the "final" realizations, we note that the F-circuit requires roughly 12 times the total capacitance of the E-circuit, in spite of the fact that the initial values were almost identical. Thus, alternative designs must be carried to completion before they can be meaningfully compared. It should be noted that other practical examples exist where the F-circuit designs are dramatically more efficient than the corresponding E-circuit designs.

As a final step, Monte Carlo simulations on the two circuits were carried out, assuming each capacitor to have a flat, independent ± 1 percent tolerance. It should be pointed out that independent 1-percent capacitor tolerances represent a pessimistic estimate in view of today's technology. Since capacitor deviations, whether they are due to manufacturing tolerances, temperature variations, or aging, are highly correlated, the capacitor ratios are recognized to be achievable[6,7] with considerably better precision. These results, given in Table V, show both circuits to be excellent, with the E-circuit being slightly superior. Note that σ_1 is the absolute standard deviation at 1 Hz, while σ_{1700} is the standard deviation of the relative gain at 1700 Hz with respect to 1 Hz.

Table V—Low-pass notch realization

Capacitor (pf)	E-Circuit			F-Circuit		
	Initial	Dynamic Range Adjusted	Final	Initial	Dynamic Range Adjusted	Final
A	1.0000	0.08308	1.0000	1.0000	0.08395	30.1895
B	1.0000	1.0000	12.0365	1.0000	1.0000	359.629
C	0.00694	0.00694	2.5035	0.00696	0.00696	1.0000
D	1.0000	0.08308	29.9613	1.0000	0.08395	12.0591
E	0.00277	0.00277	1.0000	—	—	—
F	—	—	—	0.00278	0.00278	1.0000
G	0.00694	0.00694	2.5035	0.00696	0.00696	1.0000
H	—	—	—	—	—	—
I	—	—	—	—	—	—
J	—	—	—	—	—	—
$K(I = J)$	0.89093	0.89093	10.7238	0.89340	0.89340	321.293
ΣC (pF)	—	—	59.7	—	—	726.1
σ_1 (dB)	—	—	0.068	—	—	0.068
σ_{1700} (dB)	—	—	1.233	—	—	1.271

4.2 High Q bandpass circuits

This example demonstrates the versatility of the topology and examines the various tradeoffs this versatility provides. As noted in the previous sections and highlighted in Tables I through IV, we have the following degrees of freedom in realizing a bandpass active-sc biquad.

(*i*) The transfer function; namely, BP 00, BP 01, or BP 10, as shown in Table I.

(*ii*) The circuit realization; namely, the *E*- or *F*-circuits.

(*iii*) The output port; namely, T_E or T'_E for the *E*-circuit and T_F or T'_F for the *F*-circuit.

Using the "simple" solutions given in Tables II through IV, these freedoms yield 12 different design possibilities for a bandpass biquad realization. In selecting a design from these 12 possibilities, we adopt the following criterion: The circuit must meet all frequency domain requirements within acceptable tolerances. The circuit that satisfies this criterion, while requiring an estimated minimum silicon area for its realization, is in our view the best design. The primary factor that determines the required silicon area is total capacitance. Of secondary importance are the number of capacitors and the number of switches, i.e., an unswitched capacitor consumes less area than a switched capacitor of the same capacitance value. Let us now consider the various design possibilities in view of these considerations.

The transfer function to be realized will be based on the following *s*-domain transfer function:

$$T(s) = \frac{2027.9s}{s^2 + 641.28s + (1.0528 \times 10^8)}, \tag{44}$$

which possesses a center frequency $f_o = 1633$ Hz, a quality factor $Q = 16$, and a peak gain of 10 dB at f_o.

For the active-sc design, the assumed sampling frequency is 8 kHz, i.e., $T_s = 125$ μs. One method for obtaining the *z*-domain transfer function is the application of the bilinear transform given by (23) to the prewarped *s*-domain transfer function. The prewarped *s*-domain function is obtained by adjusting the desired 3-dB frequencies f_l and f_h according to the relation[11]

$$\tilde{f}_{l,h} = \frac{1}{\pi T_s} \tan(\pi f_{l,h} T_s), \tag{45}$$

where $\tilde{f}_{l,h}$ denotes the prewarped 3-dB frequencies. Upon calculating $\tilde{f}_l$ and $\tilde{f}_h$, the following prewarped transfer function is determined:

$$\tilde{T}(\tilde{s}) = \frac{3159.2\tilde{s}}{\tilde{s}^2 + 999.0289\tilde{s} + (1.4285 \times 10^8)}. \tag{46}$$

Substituting for the prewarped complex frequency variable $\bar{s}$ in (46), the bilinear transform (23) yields the following BP 10 z-domain transfer function:

$$T(z) = \frac{0.1219(1 - z^{-1})(1 + z^{-1})}{1 - 0.5455z^{-1} + 0.9229z^{-2}}. \tag{47}$$

In accordance with the synthesis procedures given in Section III and in Tables II through IV, the four possible "simple" BP 10 designs were evaluated. The total capacitance required for each of these realizations is listed in Table VI. The capacitance values were scaled in the same manner as described in the previous example. As noted in Section II, switched capacitors, G and H, when equal, can be replaced by a single unswitched capacitor. All four designs were simulated on CAPECOD[20,21] to verify the response and to determine their statistical behavior. The Monte Carlo simulations were carried out at the 1633-Hz peak frequency, assuming each capacitor to have a flat, independent ±1 percent tolerance. Note that σ_{1633} is the standard deviation of the absolute gain at 1633 Hz. The results of these simulations are listed in Table VI.

Comparing the four designs, it is apparent that the F-circuit, using either T_F or T'_F, requires less capacitance and is less sensitive than either of the E-circuit designs. The 0.25-dB standard deviation for the F designs indicates the good stability of these circuits. Although the T'_F design consumes slightly less capacitance (~3 pF) than the T_F design, it requires one more capacitor and four additional switches. Depending on the layout, the additional capacitor, switches, and connections can more than offset the total capacitance advantage. With this reasoning, we are inclined to recommend the T_F design.

As noted earlier, one of our degrees of freedom is the choice of the BP transfer function. Exercising this freedom, as we shall soon demonstrate, can significantly impact the character of the designed circuit. Alternative realizations can be obtained by altering the z-domain transfer function in (47) to achieve a BP 00 function. An appropriate BP 00 function is obtained from (47) by removing the zero at one-half the sampling rate and adjusting gain K from 0.1219 to 0.1953 to preserve the desired 10-dB peak gain. The desired BP 00 transfer function is then

Table VI—Comparison of BP 10 and BP 00 biquad realizations

Case		E-Circuit (T_E)	F-Circuit (T_F)	E-Circuit (T'_E)	F-Circuit T'_F)
(1) BP 10, 10-dB	ΣC (pF)	55.0	51.2	75.1	48.3
gain at 1633 Hz	σ_{1633} (dB)	0.2738	0.2524	0.9932	0.2569
(2) BP 00, 10-dB	ΣC (pF)	46.7	32.7	39.6	32.8
gain at 1633 Hz	σ_{1633} (dB)	0.2852	0.2554	0.2833	0.2570

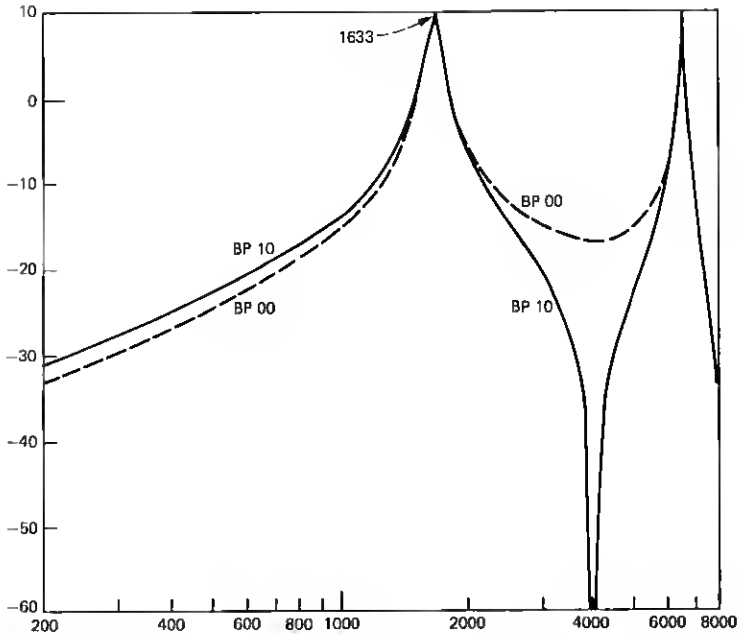


Fig. 8.—Frequency responses for the BP 10 and BP 00 designs with $Q = 16$ and $f_0 = 1633$ Hz.

$$T(z) = \frac{0.1953(1 - z^{-1})}{1 - 0.5455z^{-1} + 0.9229z^{-2}}. \tag{48}$$

Before carrying out the circuit designs, let us examine the frequency domain behavior of (48). The frequency responses for both the BP 10 and BP 00 transfer functions are plotted in Fig. 8. The BP 00 response is seen to be equivalent to the BP 10 response except for frequencies near 4000 Hz, where (47) possesses a zero. In any event, the BP 00 response was considered adequate. The appropriately scaled E- and F-circuit designs are listed in Table VI. In contrast to the first example, the F-circuit designs are seen to require less total capacitance and to be less sensitive than the E-circuit designs. More important, however, is the comparison between the BP 10 and the BP 00 designs. The BP 00 F-circuit designs are seen to require about 20 pF less total capacitance while sacrificing nothing. As far as the F-circuit BP 00 designs are concerned, our inclination is to recommend the T'_F design which requires four fewer switches than the T_F design.

V. CONCLUSIONS

Two closely related two-amplifier, active-SC filter topologies have been presented. These circuits have been constructed so that they are immune to parasitic capacitances normally present in SC networks.

The first topology, the E-circuit, has been shown to permit the realization of arbitrary stable z-domain biquadratic transfer functions at either of its two outputs. The second topology, the F-circuit, has been shown to be only slightly less general in that only certain unimportant pole pairs (real poles of opposite signs) are not realizable. A complete set of synthesis equations is presented for both of these circuits. Since every desired biquadratic transfer function has at least four alternative realizations, the designer can choose among these to best satisfy his economic and sensitivity requirements. If the "simple solutions" given in the tables do not satisfy his requirements, many other possible realizations also exist, especially if an LP or BP is being designed.

Several examples have been given to demonstrate the design process and to highlight the many degrees of freedom these biquad topologies provide.

APPENDIX

In the text, we have assumed that the input signal is sampled and held for the full clock period. While this assumption simplifies the analysis, it is by no means necessary. Thus, consider the more general case where the clock period is still T_s but the desired input signal is sampled and held only for the interval τ_e, ($\tau_e < T_s$). The subscript "e" here is meant to imply the even phase of the clock period. The odd phase of the clock period is referred to as τ_o ($\tau_o = T_s - \tau_e$). The input during this phase is assumed to be "undesirable." These concepts are also shown in Fig. 9.

In certain special cases, the circuits of Fig. 1 will continue to perform correctly even with this less restricted class of inputs. This happens whenever $H = 0$ and $J = 0$. This is readily confirmed by observing that the input voltage during τ_o is coupled into the circuit only via the two capacitors H and J. When these are both absent, the input during the odd clock phase is simply not "seen" by the circuit.

In general, however, the circuits of Fig. 1 must be modified by reversing the switch phasings of the switched capacitors A, H, and I. The resulting active-SC circuits are shown in Fig. 10. Note that the topology is so arranged that only the input during the even phase is coupled into the circuit. Thus, the input during the odd phase is again immaterial. One slight constraint on the operation of this circuit is that now the "correct" output is also only obtained during the even phase. Thus, if a fully held output signal is desired, the circuits of Fig. 10 will have to be followed by a suitable sample-and-hold circuit.

The proof of the above statement is most conveniently obtained by using the equivalent circuit techniques given in Ref. 16. For convenience in analysis, the duty cycle is assumed to be 50 percent, i.e., $\tau_e =$

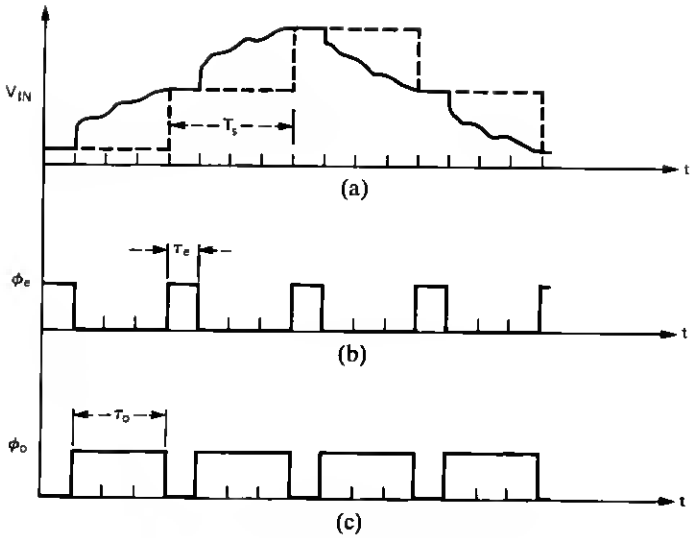


Fig. 9—Waveforms when input is not fully held.

$\tau_o = \frac{1}{2}T_s$; however, this does not detract from the generality of the results.

The equivalent circuit given in Fig. 11 can be readily constructed by substituting the equivalent circuits[16] for each SC element and operational amplifier in the circuit schematic given in Fig. 10. Due to the new switch phasings, V_{in}^{o} does not enter the filter. Writing nodal charge equations at the four virtual ground nodes of this circuit yields the following system of equations:

$$GV_{in}^{e} + DV'^{e} - Dz^{-1/2}V'^{o} + (C + E)V^{e} - Ez^{-1/2}V^{o} = 0, \quad (49)$$

$$-Hz^{-1/2}V_{in}^{e} + DV'^{o} - Dz^{-1/2}V'^{e} + EV^{o} - Ez^{-1/2}V^{e} = 0, \quad (50)$$

$$IV_{in}^{e} + (F + B)V^{e} - Bz^{-1/2}V^{o} = 0, \quad (51)$$

and

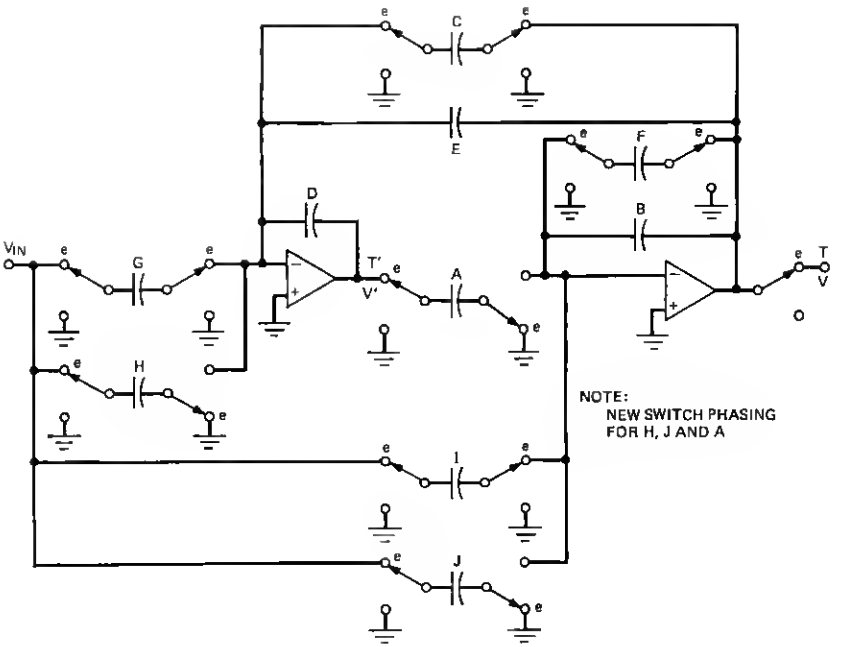
$$Jz^{-1/2}V_{in}^{e} - Az^{-1/2}V'^{e} + BV^{o} - Bz^{-1/2}V^{e} = 0. \quad (52)$$

Algebraically eliminating V^{o} and V'^{o} from these equations results in the following pair of equations:

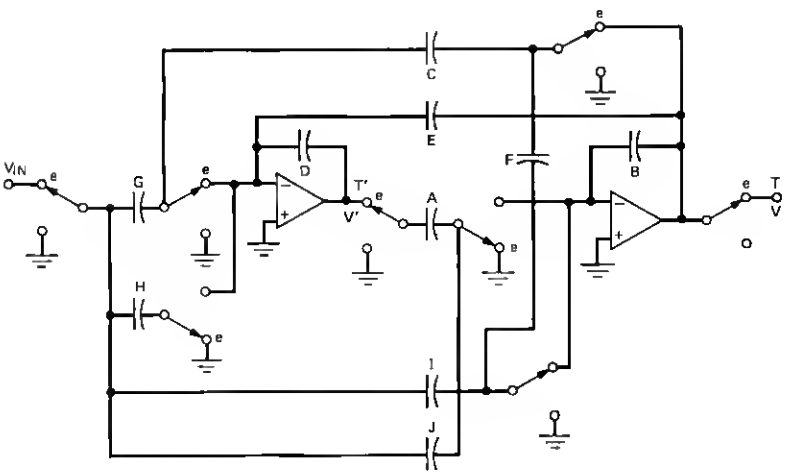
$$(I - Jz^{-1})V_{in}^{e} + (F + B - Bz^{-1})V^{e} - Az^{-1}V'^{e} = 0 \quad (53)$$

and

$$(G - Hz^{-1})V_{in}^{e} + D(1 - z^{-1})V'^{e} + (C + E - Ez^{-1})V^{e} = 0. \quad (54)$$



(a)



(b)

Fig. 10—(a) General biquad topology for input signals which are not held constant over the full clock period. (b) General biquad topology for input signals which are not held constant over the full clock period (minimum switch configuration).

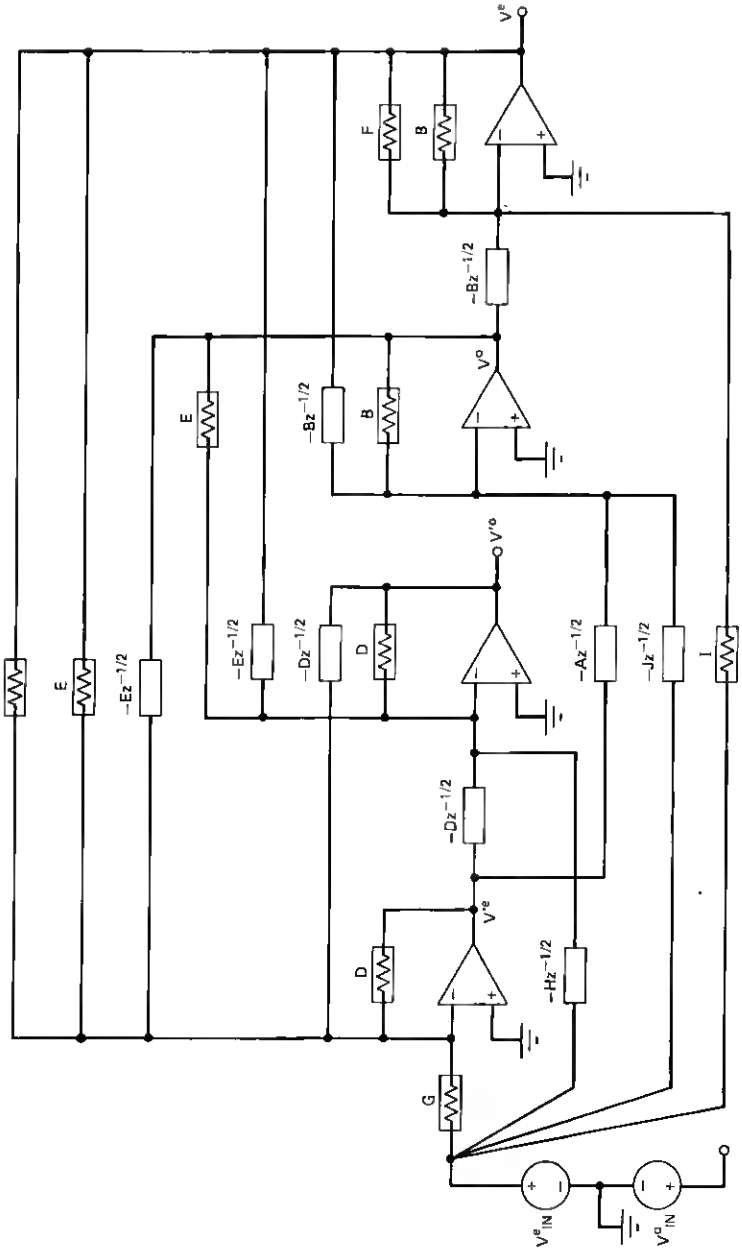


Fig. 11—z-domain equivalent circuit for the active sc biquad in Fig. 10.

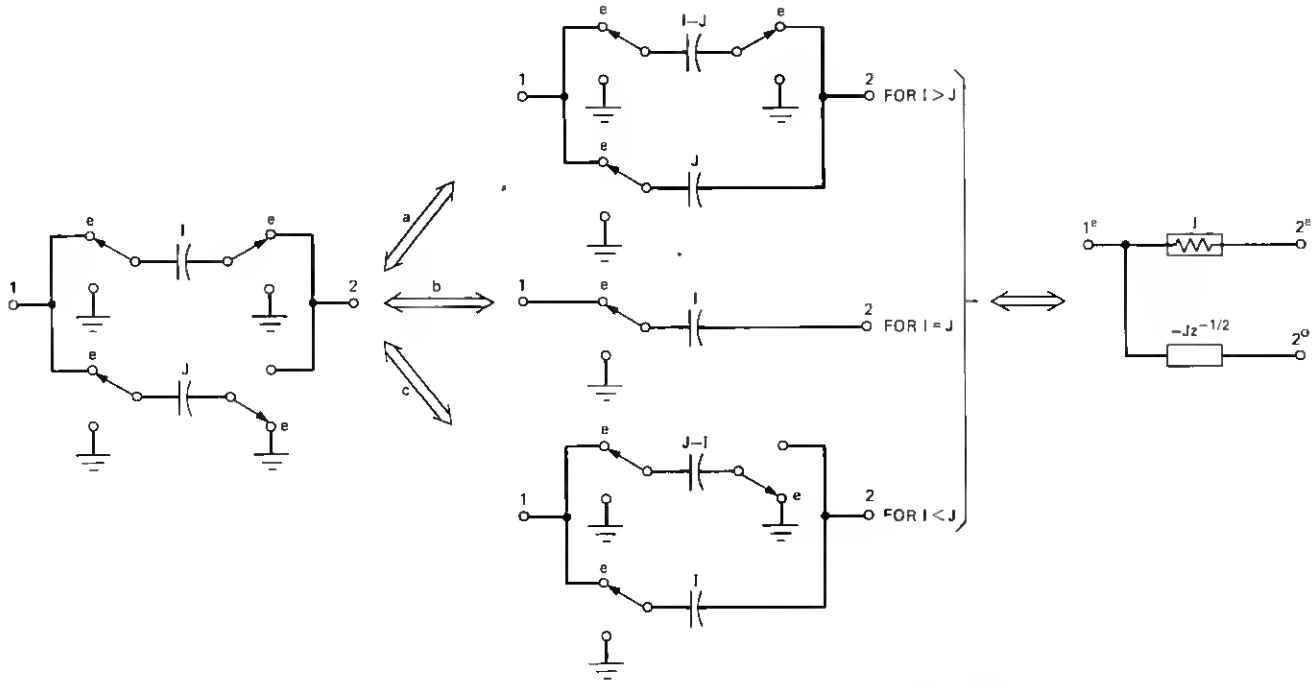


Fig. 12—sc element transformations for the biquad in Fig. 10 (ports 1 and 2 are assumed to be buffered).

Equations (53) and (54) can be readily verified to be the nodal equations which characterize the equivalent circuit given in Fig. 4. Thus, during the even phase the transfer functions will again be those given in (5) and (6), thus proving our contention. Note carefully, however, that, during the odd phase, the transfer functions which relate V_{in}^{e} to V^{o} and V'^{o} are quite different from those which characterize the even phase operation. In fact, we can express the two odd outputs (V^{o} and V'^{o}) as functions of the even outputs (V^{e} and V'^{e}) and the even input (V_{in}^{e}); i.e.,

$$V^{o} = z^{1/2}\left[\left(1 + \frac{F}{B}\right)V^{e} + \frac{I}{B}\,V_{in}^{e}\right] \tag{55}$$

and

$$V'^{o} = z^{1/2}\left[z^{-1}V'^{e} - \frac{E}{D}\left(1 + \frac{F}{B} - z^{-1}\right)V^{e} + \left(\frac{EI}{DB} - \frac{H}{D}\,z^{-1}\right)V_{in}^{e}\right]. \tag{56}$$

It is noted that, for $F = I = 0$, $V^{e} = z^{-1/2}V^{o}$; thus, V is held for the full clock period. On the other hand, when $E = H = 0$, V' is held for the full clock period. Thus, in some special cases, at least, a fully held output can be obtained. Finally, SC-element equivalences similar to those given in Fig. 5 can be used to reduce sensitivity and/or total capacitance. These element equivalences and their common z-domain equivalent circuit are given in Fig. 12. As in Fig. 5, these equivalences are based on the assumption that port 1 is voltage-driven and port 2 is connected to an operational-amplifier virtual ground.

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